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Term	Documents
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<u>L31</u>	L30 and l6	81	<u>L31</u>
<u>L30</u>	L25 and branch\$5 near6 (predict\$5 or guess\$3 or speculat\$5)	128	<u>L30</u>
<u>L29</u>	L25 and l6	147	<u>L29</u>
<u>L28</u>	L25 and l7	9	<u>L28</u>
<u>L27</u>	L25 and l8	0	<u>L27</u>
<u>L26</u>	L25 and l5	0	<u>L26</u>
<u>L25</u>	hardware near8 (multi or plur\$7 or two or second or multipl\$7) near5 thread\$3	612	<u>L25</u>
<u>L24</u>	(thread\$3 or multi near1 thread\$3) and l1	0	<u>L24</u>
<u>L23</u>	L1 and (machine\$1 or assembl\$4 or compil\$7 or link\$5)	1	<u>L23</u>
<u>L22</u>	L1 and assembl\$4	0	<u>L22</u>
<u>L21</u>	L18 and l8	12	<u>L21</u>

<u>L20</u>	L18 and l7	2	<u>L20</u>
<u>L19</u>	L18 and l6	36	<u>L19</u>
<u>L18</u>	L17 and l5	40	<u>L18</u>
<u>L17</u>	(token\$1 or value\$1 or field\$1 or flag\$1 or bit\$ or specif\$5) near8 branch\$5 near6 (predict\$5 or guess\$3 or speculat\$5)	1464	<u>L17</u>
<u>L16</u>	l5 and l3	2	<u>L16</u>
<u>L15</u>	l5 and l2	2	<u>L15</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L14</u>	l2 and l8	4	<u>L14</u>
<u>L13</u>	l2 and l7	2	<u>L13</u>
<u>L12</u>	l2 and l6	17	<u>L12</u>
<u>L11</u>	l5 and l8	17	<u>L11</u>
<u>L10</u>	l5 and l7	9	<u>L10</u>
<u>L9</u>	l5 and l6	92	<u>L9</u>
<u>L8</u>	(712/239)[CCLS]	421	<u>L8</u>
<u>L7</u>	(712/208-213, 233-240)![CCLS]	1366	<u>L7</u>
<u>L6</u>	(712/2-300)[CCLS]	11496	<u>L6</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L5</u>	(number ) near8 instruction\$1 near8 (after or subsequent\$2 or sequnc\$3 or target) near8 branch\$3 near8 execut\$5	162	<u>L5</u>
<u>L4</u>	L3 not l2	4	<u>L4</u>
<u>L3</u>	(token\$1 or value\$1 or field\$1 or flag\$1 or bit\$ or specif\$5) near8 branch\$5 near6 guess\$3	28	<u>L3</u>
<u>L2</u>	(token\$1 or value\$1 or field\$1 or flag\$1 or bit\$) near8 branch\$5 near6 guess\$3	24	<u>L2</u>
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<u>L1</u>	5724563.pn.	1	<u>L1</u>

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## » Key

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IEEE CNF	IEEE Conference Proceeding
IEEE CNF	IEEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information:

- ☐ **1. Reducing the branch penalty in pipelined processors**  
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 Digital Object Identifier 10.1109/2.68  
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- ☐ **2. SPARC64: a 64-b 64-active-instruction out-of-order-execution MCM processor**  
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 Volume 30, Issue 11, Nov. 1995 Page(s):1215 - 1226  
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- ☐ **3. Control flow prediction schemes for wide-issue superscalar processors**  
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- ☐ **4. Out-of-order commit processors**  
 Cristal, A.; Ortega, D.; Llosa, J.; Valero, M.;  
 High Performance Computer Architecture, 2004. HPCA-10. Proceedings. 10th International Sympo  
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[AbstractPlus](#) | Full Text: [PDF](#)(320 KB) IEEE CNF
- ☐ **5. FSEL - selective predicated execution for a configurable DSP core**  
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**7. Branch classification to control instruction fetch in simultaneous multithreaded architecture**

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Innovative Architecture for Future Generation High-Performance Processors and Systems, 2002. In

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**10. Instruction flow-based front-end throttling for power-aware high-performance processors**

Baniasadi, A.; Moshovos, A.;

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6-7 Aug. 2001 Page(s):16 - 21

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**14. Control flow prediction with unbalanced tree-like subgraphs**

Toone, B.R.; Franklin, M.;

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**15. Operating system impact on trace-driven simulation**

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**19. The effect of speculative execution on cache performance**

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